Arguments/Remarks:

Applicants thank Examiner Chung for the careful examination of this application and the clear explanation of the claim rejections. In response to the Office Action of November 30, 2005, applicants reply as follows:

Claim 1

Claim 1 describes a method of testing a mixed signal semiconductor device. The method includes the following steps:

a executing a first test for the at least one mixed signal semiconductor device;

b preparing execution of a second test for the at least one mixed signal semiconductor device concurrently with the executing of the first test;

c processing test data resulting from the first test; and

d executing the second test concurrently with the processing of the test data.

The Office Action rejects claim 1 as being anticipated by the Kamiya patent (4,672,534). The Office Action asserted that in lines 47-64 of column 1 and lines 10-19 of column 6, the Kamiya patent discloses a method comprising the steps of:

> Executing a first test for the at least one mixed signal semiconductor device;
>
> Preparing execution of a second test ...;
>
> Processing test data resulting from the first test; and
>
> Executing the second test concurrently with the processing of the test data.[1]

Applicants copy the cited paragraphs in the Kamiya patent below:

[1] Office Action of Nov. 30, 2005, ¶2.

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> The integrated circuit device of the present invention is characterized by comprising, in addition to a first ROM for storing an applications program for the CPU, a second ROM having an address space which is addressed in common with the first ROM and stores a test program, and a test control unit for expanding the address space of the first and second ROMS in a software manner. In the testing mode, the test control unit is responsive to an externally applied test control signal to couple the second ROM to the CPU so that the test program is executed. By executing the test program, the first ROM is coupled to the CPU so that a part of the applications program stored in the first ROM and externally designated is executed. When the execution of the applications program is completed, the second ROM is coupled to the CPU again so as to execute the test program for comparing execution results of the applications program with expected values.[2]
>
> * * *
>
> ...said second selector being controlled by said data processing unit to couple to said address register said increment circuit when the first test program is executed, said branch register when the second instruction is loaded in said instruction register, or said interrupt table when the execution of the application program instructions is completed so that said counter produces the output signal to initiate the execution of the second test program.[3]

The first paragraph cited in the Office Action discloses an integrated circuit device that has a first ROM for storing an applications program and a second ROM for storing a test program. The test program is operative when the device is in a "testing mode." In the testing mode, the CPU first executes a portion of the applications program; when this execution is completed, the second ROM is coupled to the CPU so it can execute the test program.

The second paragraph cited in the Office Action is a clause in the only claim in the Kamiya patent. It discloses a selector (said second selector) that is controlled by a CPU to couple an address register to three possible components:

1. a increment circuit when a first test program is executed;
2. a branch register when a second instruction is loaded in an instruction register; or

[2] US 4,672,534, col. 1, ll. 47-64.
[3] Ibid. col. 6, ll. 10-19.

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3. an interrupt table when the execution of a application program instructions is completed so that a counter produces an output signal to initiate the execution of a second test program.

No where in the cited two paragraphs can one find element (a), (b), (c), or (d) in claim 1 of this application. Applicants respectfully submit that because the cited reference does not disclose all the elements in claim 1, it does not anticipate claim 1 and claim 1 stands patentable over the cited reference.

Claims 2-11

Claims 2-11 properly depend from patentable claim 1 with additional elements of limitation of which not all are disclosed in the cited references. They stand patentable at least by virtue of their dependence.

Claim 12

Claim 12 describes an apparatus that includes a processor configured to perform the following four tasks:

a execute a first test for the at least one mixed signal semiconductor device;

b prepare execution of a second test for the at least one mixed signal semiconductor device concurrently with the executing of the first test;

c process test data resulting from the first test; and

d execute the second test concurrently with the processing of the test data.

The Office Action rejects claim 12 "under similar rationale as set forth in claims 1-6, 8-11."[4]

For the same reason presented relating to claim 1, applicants respectfully submit that the Kamiya patent does not disclose either element (a), (b), (c), or (d)

[4] The Office Action of Nov. 30, 2005, ¶ 2, ll. 17-18.

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of claim 12. And because the Kamiya patent does not anticipate claim 12, claim 12 stands patentable over the Kamiya patent.

Claims 13-24

Claims 13-24 properly depend from patentable claim 12 with additional elements of limitation of which not all are disclosed in the cited references. They stand patentable at least by virtue of their dependence.

Claim 25

Claim 25 describes a computer program product that includes a set of instructions configured to enable a mixed signal semiconductor device test system to perform the following tasks:

a execute a first test for at least one mixed signal semiconductor device;

b prepare execution of a second test for the at least one mixed signal semiconductor device concurrently with the executing of the first test;

c process test data resulting from the first test; and

d execute the second test concurrently with the processing of the test data.

The Office Action rejects claim 25 "under the same rationale as set forth in claims 1-6, 8-11."[5]

For the same reason presented relating to claims 1 and 12, applicants respectfully submit that the Kamiya patent does not disclose either element (a), (b), (c), or (d) of claim 25. And because the Kamiya patent does not anticipate claim 25, claim 25 stands patentable over the Kamiya patent.

[5] Ibid.

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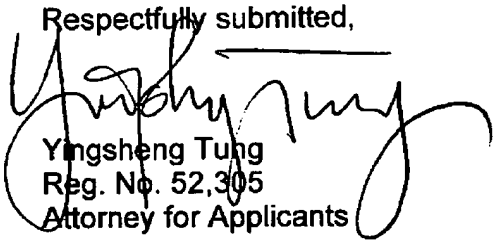
Claims 26-34

Claims 26-34 properly depend from patentable claim 25 with additional elements of limitation of which not all are disclosed in the cited references. They stand patentable at least by virtue of their dependence.

In summary, applicants respectfully submit that this application is in allowable form and all pending claims 1-34 distinguish over the cited reference and stand patentable. Applicants respectfully request further examination of this application and timely allowance of all pending claims.

Respectfully submitted,



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